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AN EFFICIENT VLSI EXECUTION OF DATA TRANSMISSION ERROR DETECTION BASED GOLAY CODE AND EXTENDED GOLAY CODE

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ABSTRACT

Channel coding is commonly incorporated to obtain sufficient reception quality in wireless mobile communications transceiver to counter channel degradation due to inter-symbol interference, multipath dispersion, and thermal noise induced by electronic circuit devices. High speed and high throughput hardware for encoder and decoder could be useful in communication field. Due to the channel achieving property, the GOLAY code has become one of the most favorable error-correcting codes. As the GOLAY code achieves the property asymptotically, however, it should be long enough to have a good error-correcting performance. In this project, a new algorithm has been proposed for CRC based encoding scheme, which devoids of any linear feedback shift registers (LFSR). In addition, efficient architectures have been proposed for both Golay encoder and decoder, which outperform the existing architectures in terms of speed and throughput. The proposed architectures power was tested on Artex-4 Xilinx power estimator. Although the CRC encoder and decoder is intuitive and easy to implement, and to reduce the huge hardware complexity required. The proposed method it improve the transmission system performance level. In this architecture, our work is to design a GOLAY code based encoder and decoder architecture using CRC processing technique. This technique is to reduce the circuit complexity for data transmission and reception process.

Keywords: *Architecture, Golay code, extended golay code, linear feedback shift register.*

I. INTRODUCTION

The Golay codes were first discovered by Golay in 1949[1]. The 23-bit Golay code is a very useful code, particularly for those applications when a parity bit is added to each word to yield a half-rate code. Among them, the Golay code was utilized to provide error control on the voyager mission. An algebraic decoding algorithm for the Golay code is given to correct the three possible errors. In 1990, another decoding approach developed is developed, called the shift-search decoding procedure. As shown, this shift-search procedure compares favorably in complexity and speed with the completely Elia decoding method. The algebraic technique is slightly faster than that of the shift-search procedure [2]. In this paper, based on the idea of, a novel reduced lookup table method is developed to decode the (23, 12, 7) Golay code. The reduced lookup table using in this algorithm consists of syndrome patterns and corresponding error patterns which only have one and two errors in the message block of the code word. The proposed method works as follows: Given a received code word r, first, the syndrome s is computed and then the weight of this syndrome w(s) is computed directly. If w(s) =0, it means no errors happened in the received code word. If w(s) $\leqq$3, it means at most three errors happened in the parity check block of the received code word. One just need to do is shifting the syndrome left k bits to form a 23-bit length word, and then the received code word minus (modulo 2) this 23-bit length word to correct the received code word If w(s) $\geqq$4, it means at least one error happened in the message block of the received code word. First, one searches if this syndrome matches the syndrome pattern listed in the reduced lookup table.

If the syndrome is in the table, it means at most 2 errors happened in the message block of the received code word, and then the received code word minus (modulo 2) the error pattern corresponding to the syndrome to correct the received code word. Second, if the syndrome is not in the table, it means there are three possible conditions: 1. one error in the parity check block two errors in the message block, 2. two errors in the parity check block one error in the message block, or 3. three errors in the message block. For 1st condition, using syndrome minus (modulo 2) syndrome pattern in the table to obtain the difference and compute the weight of this difference respectively [3]. If this weight equals to 1, it means there is one error in the parity check bit. So, shifting the difference left k bits to form a 23-bit length word, and then the received code word minus (modulo 2) this 23-bit length word and minus corresponding error pattern to correct the received code word. The proposed scheme that employs error correction codes for fault tolerant retrieval is useful in such a way that it eliminates the performance degradation of the brute force procedure.

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II. EXISTING METHOD FOR THIS ALGORITHM

A conventional fully parallel architecture for LDPC decoder was designed. The complex routing network for fully parallel architecture designed to produce the high throughput. Large VNUs and CNUs are required for fully parallel architecture. Connections between the nodes are based on the address logic rather than routing network. The proposed method is to design the partially parallel based architecture for LDPC codes and to reduce the routing congestion in network. This architecture improve the high throughput. The Golay code was presented to address error correcting phenomena. The binary Golay code (G23) is represented as (23, 12, 7), while the extended binary Golay code (G24) is as (24, 12, 8).

The extended Golay code has been used extensively in deep space network of JPL-NASA as well as in the Voyager imaging system. In addition, Golay code plays a vital role in different applications like coded excitation for a laser and ultrasound imaging due to the complete side lobe nullification property of complementary Golay pair. All these applications need generation of Golay sequence, which is fed as trigger to the laser modules [4]. However, for generating Golay code an automatic pattern generator is used, which is of very high cost. Extended Golay Code is also known as Golay code (24, 12, 8), where we have code words of length 24 bits describing the original 12-bit message [2]. The minimum Hamming distance between any two code words is 8. The 24 Golay code is an extension of the 23 Golay code. Golay code (24, 12, 8) guarantees retrieving the original data if the error occurred is three bits or less. If errors occurred in four bits there is no guarantee to recover the original data, however, it is possible, due to the fact that the decoding may result in having the original words relate to a group or another with, perhaps, the same probability. More sophisticated choice and exploitation of the structure of both a subspace and the coset representatives are demonstrated for the (24, 12) Golay code, yielding a computational gain factor of about 2 with respect to previous methods. A ternary single-check version of the Wagner rule is applied for efficient soft decoding of the (12, 6) ternary Golay code [10]. An algorithm for maximum-likelihood soft-decision decoding of the binary (24, 12, 8) Golay code is presented. The algorithm involves projecting the code words of the binary Golay code onto the code words of the (6, 3, 4) code over GF (4)-the hex code. The complexity of the proposed algorithm is at most 651 real operations. Along similar lines, the tetra code may be employed for decoding the ternary (12, 6, 6) Golay code with only 530 real operations. Invertible sub-matrix for the redundancy part.

III. PROPOSED ALGORITHM FOR THIS MODULE

Our work is to design a GOLAY code technique based encoder and decoder using CRC methodology. This work is to increase the secure level and to optimize the circuit complexity. Proposed system is to modify the encoder and decoder data bits structure level and to add the message bit, key bit and to apply the these bits into GOLAY binary code technique[5]. This technique is to apply the majority gate analysis process and to get the final majority output bit and to add the any location in encoder architecture output data bits. To combat this problem, a hardware module programmed to yield a Golay encoded code word may be used. Golay decoder is used extensively in communication links for forward error correction. Therefore, a high speed and high throughput hardware for decoder could be useful in communication links for forward error correction. Literature surveys were conducted, which deal with encoding methods for Golay code, but these are not suitable for hardware implementation due to complexity of the algorithms. Weng and Lee invented an encoding method for Golay code comprising of a linear feedback shift register (LFSR), an overall parity bit generator, a clock doubler, a five bit counter, and some switching logic [6]. Conventionally, LFSR-based cyclic redundancy check (CRC) generation scheme is preferred for hardware implementation of encoding process. Describes a symbolic simulation-based algorithm to derive optimized Boolean equations for a parameterizable data width CRC generator/checker. The equations are then used to implement a data flow representation of the CRC circuit in VHDL. The CRC-32 polynomial, commonly used for most computer network protocol standards, was chosen to implement the algorithm. The LFSR (Linear Feedback Shift Register) circuit is implemented in VLSI (Very-Large-Scale Integration) to perform CRC calculation, which can only process one bit per cycle. Recently, parallelism in the CRC calculation becomes popular, and typically one byte or multiple bytes can be processed in parallel. In summary, this paper proposes a table-based hardware architecture for calculating CRC that offers a number of benefits. First of all, it calculates the CRC of a message in parallel to achieve better throughput. While the algorithm is based on lookup tables, it adopts multiple small tables instead of a single large table so that the overall required area remains small. A CRC value is calculated as a remainder of the modulo-2 division of the original transmitted data with a specific CRC generator polynomial [7].

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IV. ARCHITECTURE DIAGRAM

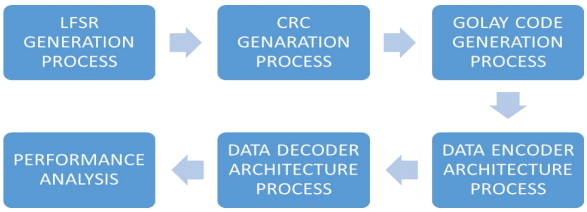

Fig 1: Architecture for proposed model

V. FLOW DIAGRAM

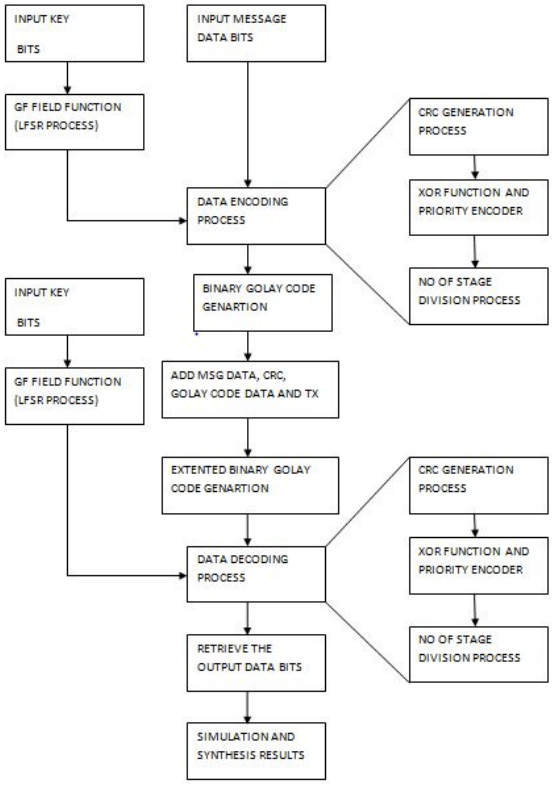

Fig 2: Flow diagram for proposed model

VI. MODULE USED

(i). LFSR GENERATION PROCESS:

Our work is to design a secure encoder and decoder architecture using GOLAY code function. So we create the key generation process based on polynomial equation. This equation is present in GALOIS field process and to update the key value in every input data bits. This process is used to improve the data secure transmission process. The pseudo random pattern generation process is mainly used to generate the pattern results based on normalized distance [8]. This technique is to obtain the pattern generation based on encode and decode circuit process function. LFSR consist of D-FF connected in cascade with the same clock applied to the entire FF to make them act like a shift register. This XOR operation introduces a new bit into the shift register.

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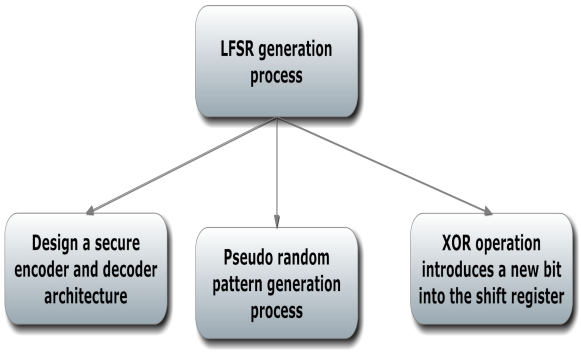

Fig 3: Flow diagram LFSR Generation process

(ii) CRC GENERATION PROCESS:

CRC methodology is a one of error detection process in data encodes and decodes process. This work is mainly focused by the division operation between input data bits and key generation bits. Our work is to modify the division operation architecture in encode and decode function. We apply the xor gate operation in subtraction process and to design a priority based encoder design. This design is to analysis the subtraction data bits and to add the no of '0' bits. This process is to reduce the overall division architecture level.

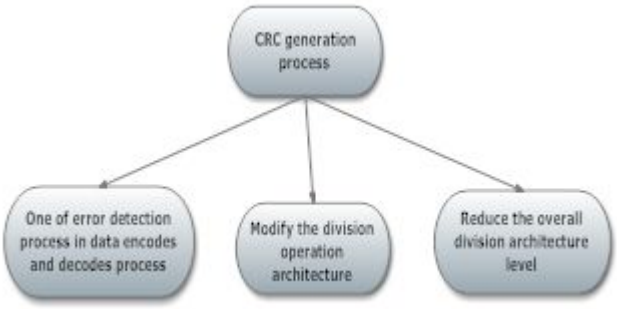

Fig 4: Flow diagram for CRC Generation process

(iii) GOLAY CODE GENERARTION PROCESS:

GOLAY code function is to add the addition key data in encoder operation. This process is to modify the data and key addition process. This function in mainly based on majority architecture design process. The 16-bit majority architecture used to the data encoding process and to modify the majority function using the BOOLEAN logic function. This logic function to optimize the Boolean equation. This equation to reduce the gate component for the 16-bit majority architecture [9].

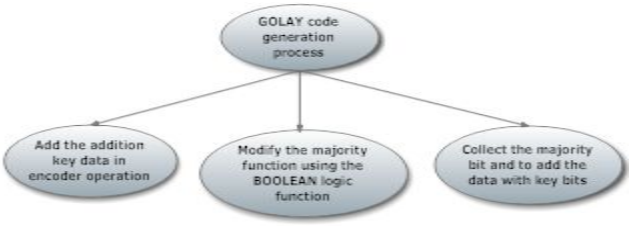

Fig 5: Flow diagram of Golay Code Generation process

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(iv) DATA ENCODER ARCHITECTURE:

Our work is design an encoder architecture using GOLAY code function. This encoder architecture is to consist of GF based LFSR equation result, CRC architecture and GOLAY code architecture. This architecture is to modify the regular encoder structure and to update the key in every data transmission processing time. Data encoder operation is add the input message bits, CRC output key bits and GOLAY code architecture based majority bits. Then to transmit the encoder architecture data bits.

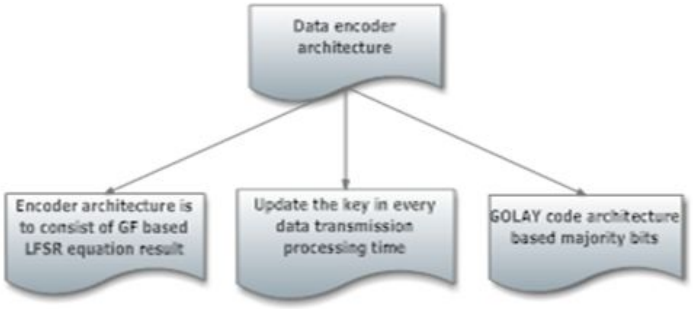

Fig 6: Flow diagram of Data Encoder Architecture

(v). DATA DECODER ARCHITECTURE:

First we collect the encoder output data bits and to modify the decoder architecture using extended GOLAY code architecture. This architecture is to analysis the overall encoder output data. Then to calculate the majority output data bits and to compare the GOLAY code architecture data bit location. Then to check the CRC key data bits. So we apply the CRC calculation process and to solve the final data bit in '0' level. Then to collect the original message data bits. The output bits are not equal to '0' level, so the error bits are present in receiving bits.

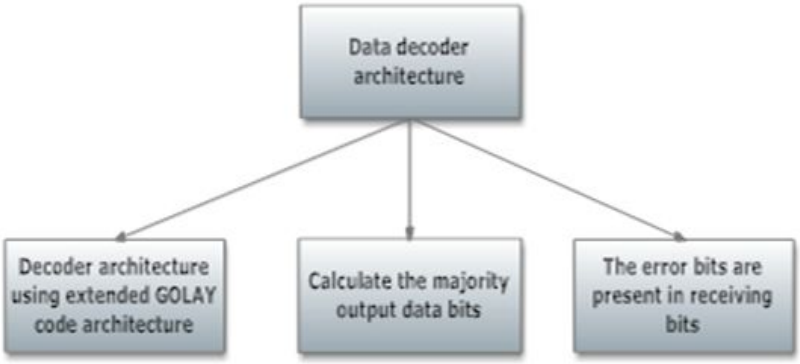

Fig 7: Flow diagram of Data Decoder Architecture

VII. SIMULATION RESULTS

The equations are then used to implement a data flow representation of the CRC circuit in VHDL. The VHDL description is subsequently synthesized to gates. The area and timing results of the hardware implementation are presented and compared with a conventional loop iteration technique. The analyzed frequency for the golay code module is 569.606 MHz. This architecture utilizes 24 slices registers out of 126800, 688 slice LUTs out of 63400 and 39 bonded IOBs out of 210.

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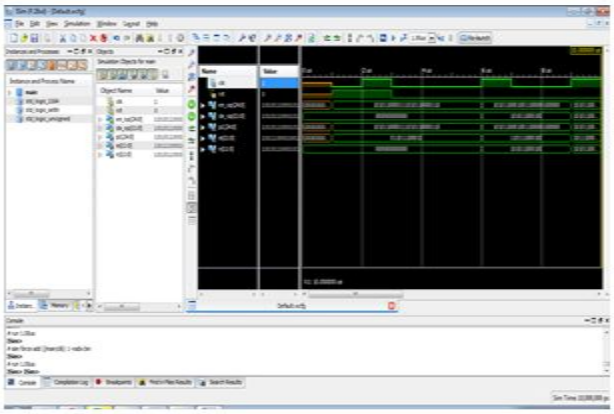

Fig 8: Simulation diagram

Table 1: Comparison Table

CONTENTS	EXISTING SYSTEM	PROPOSED SYSTEM
SLICES COUNT	972	781
LUT COUNT	333	24
DELAY TIME (ns)	2.305	1.756
CLOCK FREQUENCY (MHz)	433.657	569.606
POWER(mW)	67.9	44

VIII. CONCLUSION

Finally we design a GOLAY code based encoder and decoder architecture using CRC processing technique. This technique is to reduce the circuit complexity for data transmission and reception process compare to LDPC decoder architecture. The results obtained from simulation state that the proposed hardware architecture for encoder supersedes the conventional LFSR-based CRC generation schemes. These hardware modules for encoder and decoder can be a good candidate for various applications in high-speed communication links, photo spectroscopy, and ultrasonography.

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